Investigation of carrier selectivity and thermal stability of transition metal oxides with pre-grown SiO_x for Si solar cells Jingnan Tong¹, Kean Chern Fong¹, WenSheng Liang¹, Parvathala Narangari¹, Stephane Armand¹, Teng Choon Kho¹, Sachin Surve¹, Marco Ernst¹, Daniel Walter¹, Matthew Stocks¹, Keith McIntosh², Klaus Weber¹, and Andrew Blakers¹

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Motivation

- \Box A thin interfacial SiO_x layer (1.9-2.8 nm) is formed when deposit transition metal oxides (TMOs) on c-Si and a-Si:H (i) surfaces as a result of chemical reaction at interfaces [1-3].
- \Box The SiO_x interlayer is of great importance as it provides certain passivation and affects carrier selectivity and thermal stability [4].
- \succ This work studies the impact of an intentionally pre-grown SiO_x layer on the electronic property and thermal stability of thermally evaporated MoO_x when compared to direct deposition on c-Si.



Figure 1. Cross-sectional STEM image and EDS line scan showing a thin SiO_x layer formed when depositing MoO_v directly on c-Si. Reproduced from [3].



Figure 3. Extracted J_0 values for HF dipped and pre-oxidised p-Si (left) and n-Si (right) passivated with MoO_x and Pd

Contact Resistivity



Figure 5. Dark I-V responses of as deposited and FGA contact structures on p-Si with and without pre-grown SiO_x .



stack before and after sequential annealed in air for 10 min each at increasing temperature.

 \Box As-deposited MoO_x/Pd stack measures J_0 of ~300 fA/cm², 120-150 fA/cm² and 60 fA/cm² on samples without pre-grown SiO_x and with thermal SiO_x of 1.1 nm and 1.5 nm respectively.

 \Box Pre-grown chemical SiO_x reduces J_0 on p-Si but not on n-Si.

• Overall passivation degraded for all samples when annealed in air.



Figure 4. Change in J_0 on p-Si (left) and n-Si (right) when annealed in forming gas (FG – 5% H_2 in Ar) at 250°C.

- \Box J_o increases drastically after FGA without pre-grown SiO_x.
- \Box Except for chemical SiO_x on *p*-Si, a pre-grown SiO_x is able to

Figure 6. Extracted upper limit ρ_c values using Cox and Strack (C&S) method for as-deposited, air (left) and FG (right) annealed MoO_x on HF dipped and pre-oxidised p-Si surfaces.

- \Box As-deposited MoO_x directly on *p*-Si yields $\rho_c < 1 \text{ m}\Omega \text{cm}^2$. Naturally formed SiO_x is thicker than tunnelling threshold (~ 2 nm), indicating other charge conduction mechanism is present.
- \Box Pre-grown SiO_x increases ρ_c . Annealing in air and FG further increases ρ_c , especially when temperature is higher than 150°C.
- □ Dark *I-V* of the C&S structure on *n*-Si wafer indicates the contact rectifying, and exhibits a typical diode *I-V* curve.

□ Notably, the sample with pre-

higher junction voltage.

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grown thermal SiO_x exhibits



sustain and improve overall surface passivation after 30 min FGA at 250°C.

- \Box Though properties of MoO_x and adjacent interfaces may have changed, FGA could improve passivation provided a high quality SiO_x is present.
- Conclusion

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- \Box Pre-grown chemical and thermal SiO_x can improve overall passivation of thermally evaporated MoO_{x}/Pd and can sustain and further reduce J_{0} when annealed in FG.
- However, increased contact resistance has to be weighed against improved passivation. High-quality stable interface layer not impeding charge transport would be ideal.
- A V *n*-Si 2 Ω·cm 0.02 0.00 1.0 -0.5 0.0 0.5 Voltage (V) Figure 7. Dark I-V responses of as deposited

and FGA Cox and Strack structures on n-Si.

References

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